

REMARKS

The Office Action of January 8, 2008 has been received and its contents carefully considered.

Claims 1-21 are now pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claim Rejections - 35 U.S.C. §102(b)

Claims 1, 3-9, 11-17, 19-21 have been rejected under 35 U.S.C. §102(b) as being anticipated by Koizumi (US Patent 5,296,757). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

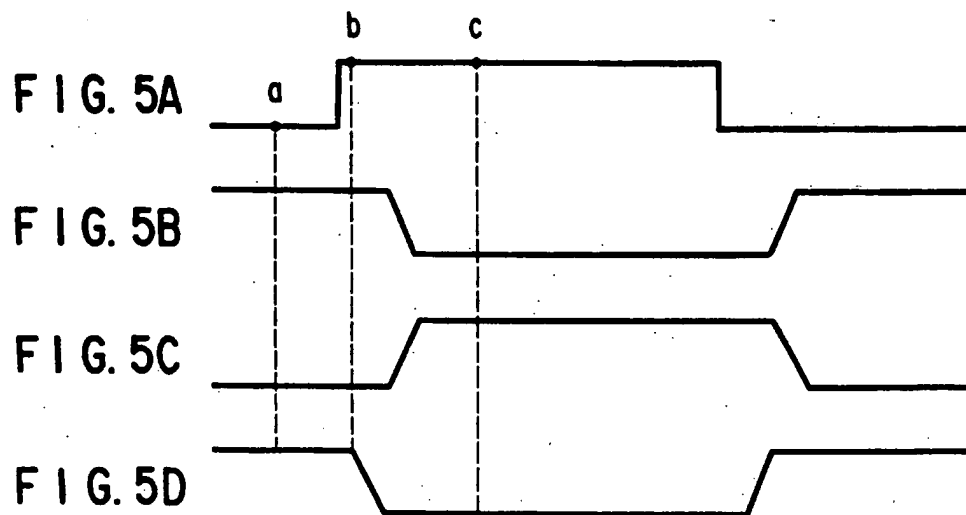
The present application is directed to a phase-interpolation circuit. Such circuits can be used in a phase-interpolation signal generating device for producing signals with the same frequency but different phases. As is set forth in Applicants' independent claim 1 (as well as in independent claims 9 and 17), a phase-interpolation circuit is for outputting a third signal according to a first clock signal and a second clock signal. In addition, the phase-interpolation circuit of claim 1 includes (among other things) a first inverter for receiving the first clock signal and a second inverter for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal. The phase-interpolation circuit includes a first controlled switch coupled to the first inverter, the second inverter, and a power source, wherein the first controlled switch is "off" when the first clock signal is in a first state, and is "on" when the first clock signal is in a second state. A second controlled switch is coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch is "on" when the first clock signal is in the first state, and is "off" when the first clock signal is in the second state. That is, the first and second controlled switches are turned on or off according to the first clock signal. In addition, the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal. For example, the output waveform of the phase

interpolation circuit is supported and illustrated by Figure 5 of the application's drawings, wherein the phase of the signal CK1-2 is determined by clock signals CK1 and CK2 and appears to be in between the clock signals CK1 and CK2.

In rejecting claim 1, the Office Action regards the signal at the input terminal A of Koizumi as the first clock signal of claim 1; PMOS transistors 22 and 23 of Koizumi as the first inverter of claim 1; and PMOS 12 and 13 transistors of Koizumi as a second inverter of claim 1; and asserts that signal C is essentially a buffered version of A, i.e. essentially the same as A. In addition, the Office Action regards the signal at the terminals B and D of Koizumi as the second clock signal and the third signal of claim 1.

It is respectfully submitted that the output circuit disclosed by Koizumi does not anticipate a phase-interpolation circuit as recited in claim 1 for the following reasons.

First, the output circuit of Koizumi does not operate as an interpolation circuit as recited in Applicants' claim 1. The circuit of Koizumi (Figure 4), relied on by the Office Action as allegedly disclosing the phase-interpolation circuit, is an output circuit (output driver) which comprises an input terminal for receiving an input signal having a predetermined logic level, an output terminal held at a potential corresponding to the logic level of the input signal (see Koizumi's abstract). That is, the output circuit 100 as shown in Koizumi's Figure 4 has only one input terminal A and one output terminal D. In addition, the signal at the output terminal is substantially an inverted version of the input signal, as indicated by Figures 5A and 5D of Koizumi (these drawings are repeated below). The Office Action asserts that signal C is essentially the same as A, which is regarded as the first clock signal, and the signal at the terminals B and D of Koizumi represent the second clock signal and the third signal of claim 1. However, with reference to Koizumi's Figures 5B, 5C and 5D, one of ordinary skilled in the art would not recognize the waveform of Figure 5D as being the interpolation of the waveforms of Figures 5B and 5C. Such a **fixed relationship between the input and output signals of Koizumi's circuit means that it does not operate as a phase-interpolation circuit** outputting a third signal according to a first clock signal and a second clock as recited in Applicants' claim 1.



Second, the failure to be a phase-interpolation circuit results from the circuit structure disclosed by Koizumi. As shown in Figure 4, the gates of MOSFETs 22 and 23 are connected to serially-connected inverters 32 and 33 and input terminal A is connected to input terminal of the inverter 32. In addition, the gates of MOSFETs 12 and 13 are connected to the output of an inverter 31 and the input terminal A is connected to input terminal of the inverter 31. The inverters 31 to 33, which act as delay elements, are designed so that node B may be in opposite phase with node C (column 3, lines 47-49). The Office Action takes the position that the signal C is essentially the same as A, which is only true in the sense of logical levels. However, the signals at nodes C and A are not the same in terms of phase, which may significantly affect the output of a phase interpolation circuit. The time delay between signals at nodes A and C due to the inverters 32 and 33, as illustrated in Figures 5A and 5C of the reference, signifies that the signal at node A cannot be regarded as the same as the signal at node C. The presence of inverters 31, 32 and 33, among other things, makes the signal at the output terminal D substantially an inverted version of the input signal at the input terminal A with a fixed phase difference, as

indicated by Figures 5A and 5D of Koizumi. **The circuit shown in Koizumi's Figure 4 therefore operates as an output driver circuit with only one input terminal and one output terminal, and would never operate as an interpolation circuit.**

Therefore, it is respectfully submitted that the output circuit disclosed by Koizumi does not anticipate a phase-interpolation circuit as recited in claim 1. Since independent claims 9 and 17 have features similar to those recited in claim 1, it is submitted that these claims, as well as the dependent claims that have been rejected, are patentably distinguishable over the cited reference and the rejection should be withdrawn.

Claim Rejections - 35 U.S.C. §102(e)

Claims 1, 2, 4-10, 12-18 and 20-21 have been rejected under 35 U.S.C. §102(e) as being anticipated by Saeki (US Patent App. Pub. No. 2002/0030525).

Saeki (US 2002/0030525 A1) has a US filing date of April 26, 2001. However, Applicants' have claimed the benefit of priority of a Taiwanese application with a filing date of February 22, 2001. A certified copy was filed in the parent of the present application (the parent application was number 10/079,866). Furthermore, attached to this Amendment is an accurate English-language translation of the priority document, as well as a statement by the translator that the translation of this certified copy of the priority document is accurate. It is respectfully submitted that the translation shows that the priority document satisfies the enablement and description requirements of 35 USC §112, first paragraph. Accordingly, it is respectfully submitted that that Saeki publication should be withdrawn as a reference.

In addition, it is noted that Saeki (US 2002/0030525 A1) claims a foreign priority date of April 27, 2000. However, MPEP §2136.03 says that the foreign priority date of a reference cannot be used to antedate an application's filing date. See also *In re Hilmer*, 359 F.2d 859, 149 USPQ 480 (CCPA 1966). Thus, it is submitted that Saeki (US 2002/0030525 A1) is not a prior art reference under 35 U.S.C. §102(e).

Claim Rejections – 35 U.S.C. §102(a)

Claims 1, 2, 4-10, 12-18 and 20-21 have been rejected under 35 U.S.C. §102(a) as being anticipated by Saeki (JP2002-14743).

The provision of 35 U.S.C. §102 sets forth:

“A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent ...”

It is noted that that the document by Saeki (JP2002-14743), which is a Japanese patent application publication document, was published on January 18, 2002. However, as discussed above, Applicants’ priority document has a filing date of February 22, 2001. Accordingly, this reference should be withdrawn, too.

Claim Rejections - 35 U.S.C. §103(a)

Claims 3, 11, and 19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Saeki (US Patent App. No. 2002/0030525). As above discussed, Applicants rely on their priority rights under 35 U.S.C. 119 to antedate this reference.

Claims 2, 10, and 18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Koizumi (US Patent No. 5,296,757). The rejection is respectively traversed. It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

Claims 2, 10, and 18 depend from independent claims 1, 9 and 17 respectively. In to the discussion of patentability of claim 1, above, it was noted that Koizumi’s circuit (Figure 4), with only one input terminal and output terminal, cannot operate as an interpolation circuit. The signal at the output terminal of Koizumi’s circuit is substantially an inverted version of the input signal, as indicated by Figures 5A and 5D of Koizumi.

In rejecting claims 2, 10 and 18, the Office Action proposes a modification of the output circuit of Koizumi (Figure 4) by adding “at least one inverter to buffer the output signal D of FIG. 4 of Koizumi to prevent loading between the output signal D of Koizumi

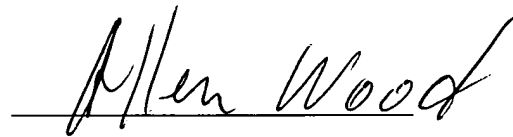
and the circuit receiving D.” However, as was discussed above, Koizumi’s circuit already includes inverters 31, 32 and 33. Furthermore, the proposed modification would merely result in an output circuit that has only one input terminal and one output terminal, with the signal at the output terminal being substantially an inverted version of the input signal, or a replica of the input signal. Such a proposed modification cannot arrive at the claimed invention, a phase-interpolation circuit, as recited in the independent claims.

Since claims 2, 10 and 18 depend from claims 1, 9 and 17 respectively, it is submitted that these claims are patentably distinguishable over the cited reference for at least the above reasons.

Conclusion:

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,

A handwritten signature in cursive script that reads "Allen Wood". The signature is written in dark ink and is positioned above a horizontal line.

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